In the Specification

Please replace the paragraph beginning on page 5 starting on line 9 with the following amended paragraph:

An IQ demodulator 113 is provided including an I mixer 115a and a Q mixer 115b. A measurement signal 119 obtained from the RF output signal 111 is split into two signals 119a and 119b, which are then input to the I and Q mixers 11 Sa and 115b. A reference signal 121 obtained from input signal 106 is split into two signals, one of which is ~~phaseshifted~~ phase-shifted 90 degrees by a phase shifter 123, resulting in reference signals 121a and 125. These signals are input to what would ordinarily be the local oscillator ports of the mixers 115a and 115a~~b~~.

Please replace the paragraph beginning on page 5 starting on line 16 with the following amended paragraph:

The mixers 115a and 115b produce respective output signals 127a and 127b, which are low-pass filtered using filters 131a and 131b and subsequently converted to digital signals using A/D converters 135a and 135b. The resulting digital I and Q signals 137a and 137b are applied to a ~~chordic~~ cordic converter 139, which produces corresponding polar signals, i.e., a phase signal 141 and an amplitude signal 143. These signals are input to the modulator 101, where they are used in accordance with an efficient update scheme described more fully hereinafter.

Please replace the paragraph beginning on page 6 starting on line 11 with the following new and amended paragraphs:

Recognizing that multiplication commutative, there is no difference whether quadrature shifting is performed on either input of mixers 115a, b.

Since Figure 1 shows the signal 125 is phase-shifted by 90 degrees relative to the input signal 106, the signal 125 may be represented as:

Please replace the paragraph beginning on page 7 in line two of the second equation with the following amended paragragh:

$$\rho' = \rho(t)$$

~~$\theta' = \phi(t)$~~

$$\theta' = \theta + PM[\rho(t)]$$

$$= \theta + \Delta\theta$$

Please replace the third paragraph beginning on page 7 with the following amended paragraph:

That is, the amplitude of the RF output signal 111 is initially the same as the desired amplitude. Also, the phase of the RF output signal 111 is ~~the same as the desired phase, set in accordance with~~ the static phase shift, θ, of the amplifier at the operating frequency and the expected distortion, PM[ρ(t)], of the amplifier as a function of amplitude variations. Note that, in order for the phase equality to be satisfied, the phase correction factor A8 applied within the

modulator must equal the actual dynamic phase modulation PM[ρ(t)] occuring within the amplifier.

Please replace the fourth paragraph beginning on page 7 with the following amended paragraph:

The foregoing description omits various details that will be apparent to one of ordinary skill in the art. For example, directional couplers (not shown) are used to obtain the measurement signal ~~111~~ 119 and the reference signal 121. In addition, signal splitters (not shown) are used to split the signals 119 and 121 into signal 119a and 119b and 121a and 121b. Moreover, signal levels at various points within the circuit may be set appropriately using attenuators, amplifiers, or a combination of the same (not shown) . For example, amplifiers will typically be used in the paths of the signals 121, 127a and 127b. In addition, a combination of attenuators (fixed and/or variable) and an amplifier will typically be used in the path of the signal 119.

Please replace the following paragraph beginning on page 9 starting on line 1 with the following amended paragraph:

The amplitude signal p is used to index a look-up-table (LUT) 209 storing correction factors ap, A9. In the illustrated embodiment, the size of the LUT 209 is kept small by using interpolation. That is, an interpolator 211 is used to form interpolated Op, A8 from those output from the LUT 209. These interpolated values are added to the p and 8 values produced by the

cordic converter 207 using summation elements 213 and 215. An output signal from the summation element ~~213~~ 215 is applied to a digital to analog converter 217 to produce an analog amplitude signal 219. This signal is amplified in a variable-gain amplifier 221 in response to a power control signal to form a final amplitude signal 223 which is applied to the amplifier. An output signal from the summation element ~~215~~ 213 is applied, in an exemplary embodiment, to a digital phase modulator 225. Of course, the digital phase modulator and the VCO 105 could be replaced in other embodiments with a conventional analog modulator (preceded by a digital to analog converter).

Please replace the following paragraph beginning on page 9 starting on line 18 with the following amended paragraph:

Adaptation is performed by calculating new Δp, $\Delta\theta$ values for a given amplitude, using the old dp, 08 values and amplitude and phase error signals 229 and 231. The old Ap, 08 values are delayed using delay elements ~~233a~~ 223a and ~~233b~~ 223b to allow for the delay from read-out of these values to signal generation and measurement.

Please replace the following paragraph beginning on page 10 starting on line 1 with the following amended paragraph:

As previously described, ~~the~~ this Cartesian feedback circuit produces information on amplitude, and on the *phase difference* ~~information~~. Accordingly, an error forming circuit 235 receives as inputs the amplitude signal 236 and phase signal 237 from the cordic converter 207

~~and the interpolated A8 signal 237 from the LUT 209~~. Once again, these signals are delayed using delay elements 238a and 238b. The amplitude signal ~~237~~ 236 is also applied to a LUT I/O circuit 239 used to control updating of the LUT 209.

Please replace the following paragraph beginning on page 10 starting on line 18 with the following amended paragraph:

Thus, there has been described a Cartesian feedback circuit operable in conjunction with a polar modulator to achieve efficient, accurate linearity correction. The Cartesian feedback circuit avoids the need for a separate local oscillator or other reference-forming circuit, minimizing complexity and minimizing errors that would otherwise be introduced into the circuit.